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PATENT
ATTORNEY DOCKET NO. 72804

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Chason et al.
Appln. No.:	10/044,777
Filed:	January 11, 2002
Title:	Semiconductor Package Device and Method
Group Art Unit:	2813
Examiner:	Dolan, J.

CERTIFICATE OF MAILING

I hereby certify that this paper is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on this date.

1/28/03
Date

Stephen S. Favakeh
Registration No. 36,798
Attorney for Applicant(s)

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Commissioner for Patents
Washington, D.C. 20231

AFFIDAVIT FOR MARC CHASON Under 37 CFR §1.131

Dear Sir:

The undersigned affiant, Marc Chason, being under oath, hereby states and declares as follows:

1. My name is Marc Chason and I am one of the inventors of the above-captioned invention entitled Semiconductor Package Device and Method.

2. We were in possession of the claimed invention prior to February 23, 2001. For example, between January 14 and 18 of 2001, we presented a paper describing the invention at the APEX Electronics Assembly Process Exhibition and Conference in San Diego, California. This presentation appears in the official proceedings of the technical conference, pertinent portions of which are attached hereto as Exhibit A.

3. The APEX paper makes reference to the use of wafer-applied underfill processes beyond that of flip-chip assembly and specifically to area array packages. For example, in this paper, we state that the disclosed concepts are applicable to the underfill of chip-scale packages and ball-grid array packages. The undersurface of a

chip-scale package comprises the "interposer" that we express in the claims of our patent application.

Further affiant sayeth not.

Submitted and sworn this 14 day of January, 2003,

Marc Chason

Marc Chason

STATE OF ILLINOIS)
) SS
COUNTY OF Cook)

I hereby certify that, before me, a Notary Public for the County and State aforementioned, personally appeared MARC CHASON, personally known to me to be the person whose name is subscribed to the within instrument, and acknowledged that he executed it.

Witness my hand and official seal.

OFFICIAL SEAL
Judith L. Thelwell
Notary Public State of Illinois
Commission No. 546350
My Commission Expires: 11/05/2005

Date: Jan. 14, 2003

Judith L Thelwell

Notary Public
My Commission Expires _____

THE APEX FILES

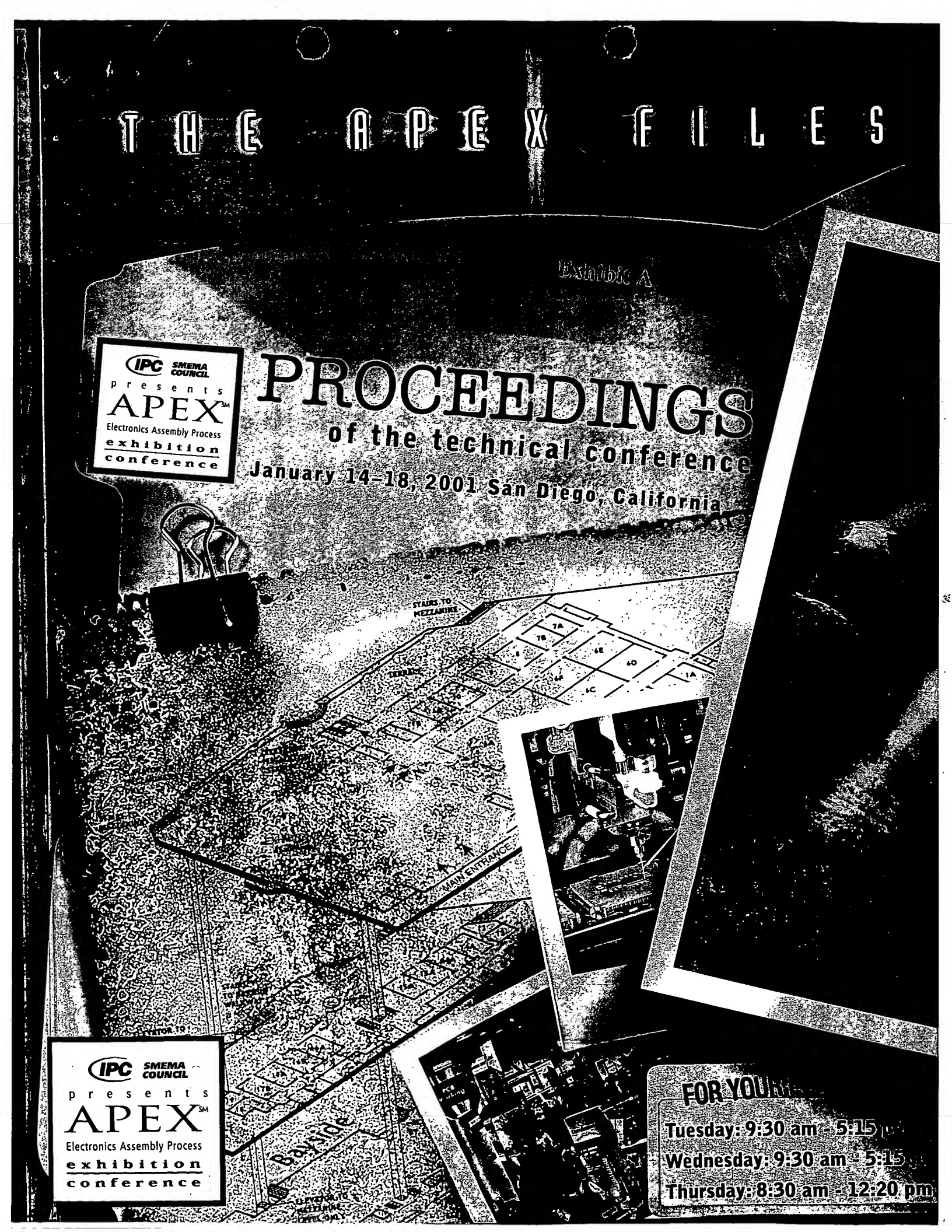
Exhibit A

IPC SMEMA COUNCIL presents APEX℠ Electronics Assembly Process exhibition conference

PROCEEDINGS

of the technical conference

January 14–18, 2001 San Diego, California



IPC SMEMA COUNCIL presents APEX℠ Electronics Assembly Process exhibition conference

FOR YOUR

Tuesday: 9:30 am - 5:15

Wednesday: 9:30 am - 5:15

Thursday: 8:30 am - 12:20 pm

CHASON

IPC SMEMA COUNCIL

presents

APEX℠

Electronics Assembly Process

exhibition

conference

PROCEEDINGS OF THE TECHNICAL PROGRAM

JANUARY 14-18, 2001

SAN DIEGO CONVENTION CENTER

SAN DIEGO, CALIFORNIA

Presented at IPC SMEMA Council APEX℠ 2001
www.GoAPEX.org

Development of Wafer Scale Applied Reworkable Fluxing Underfill For Direct Chip Attach

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Abstract

Consumer electronic products are continuously striving to have greater functionality in smaller, lighter, and less expensive packages. Flip chip and Chip Scale Packages (CSPs) are important enabling technologies for these product trends. Flip chip dies were originally attached to ceramic substrates. When this technology was transferred to less expensive organic substrates like FR-4, adding an underfill encapsulant between the die and substrate became necessary to compensate for the coefficient of thermal expansion mismatch between the organic substrate and silicon die. This necessary process step addition required Surface Mount Technology (SMT) lines desiring the flip chip technology to add space to the SMT production line for underfill dispensers and curing ovens. SMT lines were also required to add flip chip flux dispensers upstream of die placement. These flip chip floor space and capital investments plus the inability to repair underfilled parts has limited the wide scale implementation of the flip chip technology.

The National Institute of Standards and Technology Advanced Technology Program "Wafer Scale Applied Reworkable Fluxing Underfill for Direct Chip Attach" (NIST-ATP WARFU) program was established to investigate the development of a materials and manufacturing system which could make flip chip assembly transparent to SMT lines. The program is developing high performance, fluxing, reworkable underfill materials and processes for direct application of the materials to die at the wafer level. This will replace the flip chip flux application, underfill application, and cure processes with a reflowable, reworkable encapsulant application to flip chip wafers. The fully developed process will enable assembly of fine pitch (<8-mil) flip chips. The coated wafer will be cut to form single components, similar to other SMT parts. The individual die will be placed on the printed wiring board using standard pick and place equipment and reflowed with no additional processing steps required. The pre-applied material will provide the necessary fluxing activity during soldering and will serve as the underfill following curing during the reflow process. The reworkable nature of the new material system will allow in-plant rework of defective units as well as repair of field returned products.

Demonstration of the feasibility of the WARFU process requires material, process, and infrastructure development, which can best be accomplished by a vertically integrated research team. Consequently, the four year WARFU research Joint Venture (JV) was formed in April of 1999 by Auburn University, Loctite Corporation, Motorola,[1] and Jabil Circuit. This paper summarizes the research results and concludes that the proposed WARFU process is a viable transparent flip chip SMT solution with no anticipated insurmountable roadblocks.

Introduction

Direct Chip Attach (DCA) has yet to gain widespread acceptance into electronic products, due primarily to the added conversion cost associated with the capillary flow underfill and cure processes. In addition, the separate fluxing operation adds further complexity to the SMT process and reduces the flexibility of the factory, in that DCA requires additional capabilities not found in the standard SMT line. Another important consideration is the issue of repair. The DCA chip should be reworkable using the typical repair tools found in surface mount factories and be achievable under the usual constraints, i.e., surrounding components are not disturbed, the temperature must be compatible with FR4 circuit boards and the cycle time must be acceptable. Loctite[2], National Starch and Chemical[2] and Georgia Institute of Technology[2] are developing reworkable underfill materials. While these materials, when commercialized, will address the reworkability issue, they will not eliminate the non-SMT manufacturing steps in the current DCA pr cess.

The goal of the present project is to develop and implement a transparent DCA process.[5] The program will develop high performance, fluxing, reworkable underfill materials and processes for direct application of the materials to die at the wafer level. After dicing and tape and reeling, the individual die will be placed in the SMT line using standard pick and place equipment and reflowed with no additional processing steps required. The reworkable nature of the new material system will allow in-plant rework of defective units as well as repair of field returned products. The proposed process benefits relative to the present DCA assembly process will provide a significant cost advantage to assemblers who implement the process[5]. In addition, the concepts are applicable to the underfill of Chip Scale Packages and the larger Ball Grid Array packages as well since more CSPs are being underfill to enhance the mechanical integrity of the package to meet consumer requirements for portable electronic products.[7,8,9] With this recent rise in the practice of underfilling CSP's, the present work gains new importance.

Experimental materials from Loctite, including the first generation of wafer applied underfill material were used to investigate the behavior of such a package during SMT assembly. The wafer-applied underfill is Loctite's initial effort in the development of the material that is central to the WARFU concept. The material is designed to coat a bumped wafer, is b-stageable and will then completely cure within a normal SMT reflow profile.

Materials Characterization

Only limited materials characterization has been done at this stage as the materials supplied are only initial formulations provided to allow the evaluation of the assembly process.

Differential Scanning Calorimetry

Differential scanning calorimetry (DSC) tests were performed to determine the exotherm initiation temperature of the wafer applied underfill material. Figure 1 shows the resulting thermogram, with an exotherm initiation temperature of approximately 190°C. For wafer-applied materials, it is critical to have an exotherm initiation temperature above 180°C to achieve optimal DCA assembly.

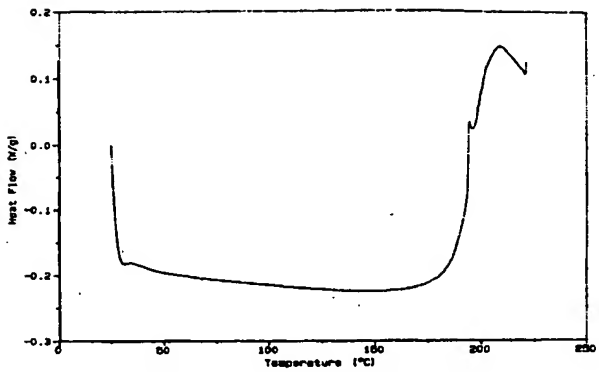


Figure 1 - Differential Scanning Calorimetry Thermogram for Wafer-Applied Underfill Material

Material Processing Studies - Cure Kinetics Studies

Dielectrometry studies were conducted (Micromet System III Dielectrometer) to determine the thermal schedules required to achieve a cured bulk material. A finite volume was dispensed on a low conductivity integrated circuit sensor. Next, the sensor was placed in an oven heated to the manufacturer's recommended cure temperature (B-staged for 1 hours at 60°C, then cured for 10 min @190°C). The dielectrometer monitored the dielectric response of the wafer applied underfill materials as a function of time. The generated data showed that the dielectric spectra were constant and no change in the loss factor over time was recorded prior to the elapse of the recommended supplier cure time.

Test method development is proceeding in an effort to reproduce a reflow spike with the dielectrometer so that the degree of cure during reflow can accurately be assessed.

Wafer Coating Processes

Finding a consistent and accurate coating method by which the material may be deposited onto the wafer is crucial to the successful implementation of WARFU. Several techniques could potentially be used for coating a bumped wafer: 1) screen/stencil printing, 2) pad printing and 3) extrusion coating.

Screen/Stencil Printing

The stencil and screen-printing processes are widely used in the electronics industry for the fabrication of printed circuit boards, flexible circuits, and other related items. The challenge in this process is the irregular surface topology presented by the solder bumps. A uniform coating thickness that does not coat the tops of the solder balls is required.

Pad Printing

Pad printing is an offset gravure printing method, where the gravure or cliché is patterned with the

artwork to be printed and ink transferred from the cliché to the part using a silicon pad. First, artwork is transferred to a stainless steel cliché plate using a photo-etch process. Ink is spread onto the cliché and a silicone pad is pressed against the cliché then lifted, with the ink adhering to the silicone pad. The part to be printed is then aligned under the pad and the pad is pressed against the part and lifted off, with the ink transferring to the part. A thin film of ink is deposited on the part, with a fine resolution and a location accuracy of +/- 2.54 E-05 m.

Pad printing has the ability to print over irregular surfaces, with the silicon pad conforming to the shape of the substrate. It is this characteristic that gives it great potential for coating a bumped wafer.

Extrusion Coating

Extrusion coating is the direct application of process fluids to a substrate via a patented, specially designed fluid pumping and delivery system. This creates a highly uniform coating over the entire substrate with virtually no waste. The extrusion coating process has been extensively used for thick film application on wide semiconductors wafers up to 300mm in diameter. This unique technique holds great potential for coating bumped wafers.

Experimental Wafer Coating

In recent work at Auburn University, the wafer-applied underfill was successfully applied on a 101.6 mm wafer. A thin uniform coating layer with clean solder balls and clean saw streets was produced. Due to the early stage of development, the coated wafers were not available for the initial assembly process work. Therefore, manual coating was adopted to demonstrate feasibility of the material systems under study.

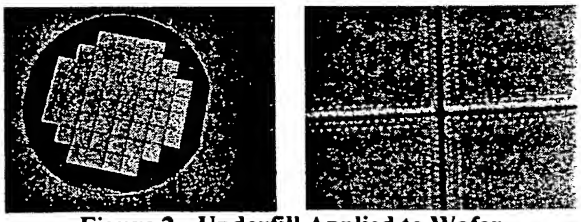


Figure 2 - Underfill Applied to Wafer

The application of underfill to single die was performed manually (Figure 3). The coated dies were then b-staged in a box oven for 1 hour at 60°C.

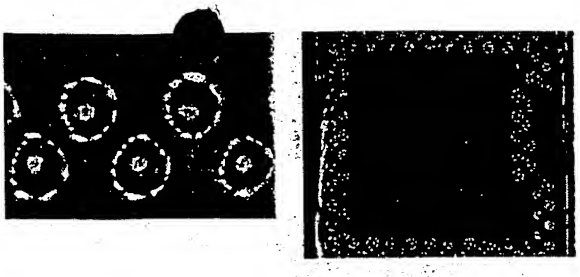


Figure 3 - Test Die Manually Coated with Wafer-Applied Underfill

The SEM micrograph of as cross-sectioned die with wafer-applied underfill shows that the manual coating technique produced a thick uniform layer of approximately 100 microns (Figure 4). A thin layer of material of approximately 10 microns is covering the tip of the solder balls. The thin layer contains fillers particles, and it was suspected that these could get embedded in the solder during reflow or otherwise influence the soldering process and affect the assembly yield. No evidence of this was found in the present experiments, however the goal is to develop a coating process that will not permit this layer to be formed on top of the bumps. Good progress to meet this goal has been made to date.

WARFU Assembly Development

Assembly experiments tested the ability to place and reflow flip chips coated with both the wafer-applied materials. Key considerations were the ability to detect the bumps on the die in placement alignment, creation of tack in the underfill on the die, formation of sufficient solder joints in reflow and formation of a fillet on the edges of the die.

Test Vehicle

For this development work a 102 mm X 102 mm uncladded FR4 PWB designed for electrical continuity measurements was used. The test vehicle had 6 DCA sites and was 0.46 mm thick. The continuity test die was 6.6 mm X 6.6 mm, and had 84 peripheral bond pads. The pitch between the 63Pb/37Sn die solder bumps was 0.356 mm. The die was approximately 0.5 mm thick and had a nitride passivation on the active side. The test vehicles were assembled on a pilot line using a qualified assembly process[9]. The line consisted of an automated flip chip placement machine (Universal GSM-1-LM) with flux dispense and dipping capabilities and a Conceptronics HVN-70 reflow furnace.

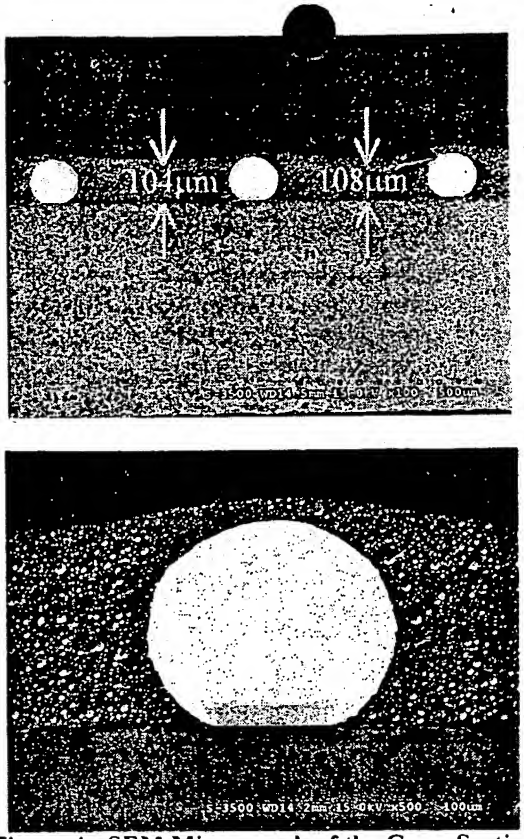


Figure 4 - SEM Micrograph of the Cross Section of Die Coated with Wafer-Applied Underfill

Vision Studies

The feasibility of using the Universal GSM robot to place flip chips coated with WARFU materials was investigated. The vision system of the Universal GSM-1-LM component placer includes a Pattern Error Correction (PEC) camera and Up Looking (UL) cameras with different resolutions. The PEC camera is the machine's downward looking inspection camera for substrate positioning and recognition. The UL camera is used for component centering and inspection, and the fine resolution UL camera enhances the machine vision capability to locate smaller die bump features.

The study showed that the vision system worked best with black-coated die that supplied the greatest contrast between the underfill and the solder bumps. Therefore, black pigment was added to the WARFU material systems.

Assembly Proces

The wafer-applied materials that are being evaluated provide fluxing action. Assemblies with this newly synthesized wafer applied underfill was carried out to demonstrate the feasibility of wafer applied underfill materials.

Earlier work has shown that a sufficient tack to hold the die in place during transfer of the assembly to the reflow furnace is required. Therefore, assembled parts were subjected to a pressure equivalent to 1000-2000 grams per die, and heated for 20-60 seconds at 60°C. All assemblies were X-rayed to ensure that the alignment was not affected with the introduction of added pressure. Next, the DCA assembly was transferred to the reflow furnace. The furnace was programmed with a typical reflow profile for eutectic Pb/Sn solder: 80 sec above 183°C and a maximum temperature of 220°C.

The assemblies displayed typical electrical conductivity of the daisy chain. In addition, the cross-sections of the flip chip joints shows good solder joint formation and good wetting (Figures 7).

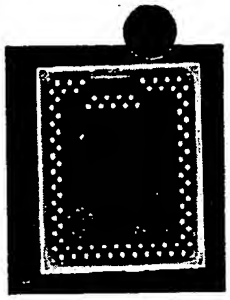
The assemblies were also inspected for the presence of fillets. While the manual coating process does not deposit an optimized amount of underfill material on the chips, fillet formation was found to occur (Figure 7). Optimization of the material viscosity, underfill volume, and placement force will be needed to consistently form adequate fillets. Also, a high-speed approach to make the underfill tacky will be developed for implementation on standard SMT pick and place machines.

Conclusion

A first generation WARFU material was received from Loctite and evaluated. The results provided convincing evidence demonstrating the feasibility of the WARFU assembly concept. Material properties will require further optimization, and the wafer coating and assembly processes will need further development. The results to date show great promise for the successful elimination of underfill operations of both Direct Chip Attach and Chip Scale Packages from Motorola SMT factories.

White Coated Die Coated die Cross-Section

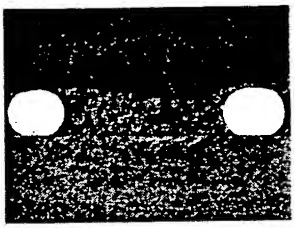
Figure 5 - Vision Studies with White Wafer-Applied Underfill Materials

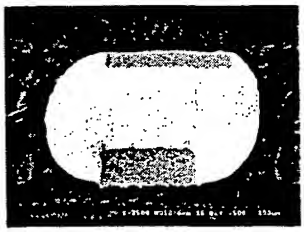


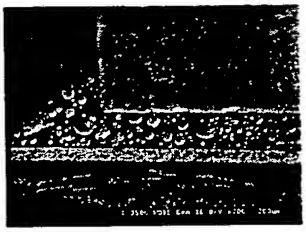
Black Coated Die

Coated die Cross-Section

Figure 6 - Vision Studies with Black Wafer-applied Underfill Materials







As coated die

Solder Joint Cross-Section

Underfill fillet formation

Figure 7 - Assembly with Wafer-applied Underfill Materials

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